plurality of flip-flop circuits each having four memory transistors and that each of the four transistors of Ishida's flip-flop circuit is connected with a corresponding bit line.

In this Action, the Examiner responds:

> As shown in figs. 8C and/or 17C, the device of Ishida comprising [sic] three (3) transistors, which respectively having [sic] word line 1 (WL1), word line 2 (WL2), and gate line 2. The transistor having GL2 includes two contact pads; one of which is connected to the ground (VSS), and the other of which is connected to the gate storage node interconnection (30b). This transistor (GL2) is clearly not connected to the bit line.

Page 3 of the Action. Applicants respectfully disagree.

Ishida's SRAM is represented by a circuit diagram shown in FIG. 1. Ishida's FIGS. 3A - 8C disclose a manufacturing method of the SRAM shown in FIG. 1. See, for example, column 16, lines 20-30, of Ishida. Specifically, Ishida's SRAM has two drive transistors Qn1 and Qn2 and two load transistors Qp1 and Qp2, which constitute one flip-flop circuit, and two switching transistors Qn3 and Qn4 that connect the four flip-flop transistors to corresponding bit lines. See, for example, column 14, line 56 - column 15, line 27, of Ishida. The "transistor (GL2)" relied upon by the Examiner is the drive transistor Qn2. See, for example, FIG. 5C of Ishida.

The circuit diagram shown in FIG. 1 of Ishida shows that the drive transistor Qn2 is connected with bit line BL2 through the switching transistor Qn4. Furthermore, FIG. 8C relied upon by the Examiner shows that the drive transistor Qn2 is connected with the bit line through the switching transistor Qn4 and Ishida's metal plug 22b. FIG. 17C, which is also relied upon by the Examiner, discloses essentially the same bit line connection as FIG. 8C. Thus, Ishida does not disclose the claim limitation that some but not all of the memory transistors are connected with corresponding bit lines by corresponding metal plugs, because all memory transistors of Ishida are connected with corresponding bit lines, without the use of the claimed metal plugs.

Claims 5 and 6 recite essentially the same bit line connection as claim 1. The rejection of claims 1, 5 and 6 under 35 USC 102(b) Ishida should be withdrawn because Ishida does not teach or suggest the claimed bit line connection.

The remaining rejection relies on Ishida and thus should be withdrawn as well because Ishida does not provide the teachings for which it is cited.

In light of the above, a Notice of Allowance is solicited.

In the event that the transmittal letter is separated from this document and the Patent and Trademark Office determines that an extension and/or other relief is required, applicants petition for any required relief including extensions of time and authorize the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952**, referencing Docket No. **606402014400**.

Respectfully submitted,

Dated: June 5, 2006

By: _____

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